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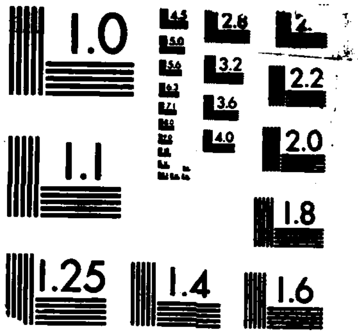

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AD-A192 702

A planar IC-compatible transferred electron device for millimeter-wave operation

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
Design rules derived from computer simulations; fabrication of devices with two different gate structures; gain of several db from 26 - 30 GHz; oscillator power of 10mw with 1.2 % efficiency at 29.7 GHz and 1mw with 0.1 % at 37 GHz using dielectric resonators.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
Computer simulations have revealed that FEDTEDs operate with high efficiencies of approx. 9 % at lower doping levels (5.10^{15} cm^{-3}) but in a very narrow range of RF/DC voltage levels. Lower efficiencies (3%-6%) are obtainable with doping levels of $2\text{-}3.10^{16}$ cm^{-3} in a much broader range of RF/DC voltages.
Experimental results obtained with a new batch of devices made from epitaxially grown layers with $N_D=2.5.10^{16}$ cm^{-3} and d=0.9µm are now very encouraging as, for the first time, broad band gain
see 2nd page

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micrometers

20 ABSTRACT continued

of several db from 26 - 30 GHz and, when loaded with a dielectric resonator output power levels of 10mw with 1.2 % efficiency at 29.7 GHz have been obtained. Both, improved device technology and optimized stripline circuitry are made responsible for the improved performance.

Future work will concentrate on pushing efficiencies up by a factor of 5 and on optimizing circuitry for 35 GHz operation.

Keywords: Field Effect Controlled Transferred Electron Devices,

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The work accomplished during the third period of the contract ending August 31, 1987 includes:

- computer simulation
- device fabrication
- design of stripline circuits
- devices operated as broadband amplifiers (26 - 30 GHz, 37 GHz)
- devices operated as oscillators (10mw, 1.2 %, 30 GHz and 1mw, 0.1 %, 37 GHz)

Computer simulation

The computer simulations of one-dimensional FECTED's have revealed that lower doped devices ($N_D \approx 5.10^{15} cm^{-3}$) operate with higher efficiencies (~9 %) than higher doped devices ($N_D \approx 2.5.10^{16} cm^{-3}$) do (~5 %). However, the range of RF and DC drain voltage levels at which the efficiency remains fairly constant (3 - 6 %) is much broader at higher doping levels suggesting that these samples will be tunable over much broader frequency bands than lower doped devices.

Another important conclusion is that maximum efficiencies are attainable at injection current levels of 110 % - 120 % of the valley current defined by $e.N_D.v_V.A$ (e = electronic charge, N_D = doping density, $v_V = 10^7 cm/s$, A = cross sectional area). The injection current level can be adjusted by adjusting the negative gate bias voltage.

The optimum distance between gate and drain is determined by the length of the depletion layer which is for the doping levels used in this simulation around 3µm. As high fields must be prevented from reaching the drain contact a safe gate to drain distance is 4 - 5µm. Larger distances add positive series resistance which reduce the efficiency somewhat. Devices with 10µm long gate to source distance, for example, exhibit efficiencies typically half as large as those 5µm long devices exhibit.

Device Fabrication

Device fabrication is now well under control. 95 % of devices made from one chip (which containes typically 60 devices) are mechanically sound. 75 % are electrically (DC-wise) sound. RF-data taken on DC-wise identical devices are

critically dependent on length and placement of bonding wires. More accurate mounting procedures have to be adopted.

Device Parameters

Due to the one-dimensionality of the computer simulation program the two-dimensional MESFET-like cathode contact structure cannot be simulated and must therefore be optimized empirically. Devices with overlapping ("grounded") gate structure as shown in Fig. 1 exhibit efficiencies only a factor of 2 - 5 smaller than theoretically predicted values. There are experimental indications that connecting the gate to an impedance level other than zero ("grounded gate") might lead to improved performance. Therefore a second type of device structure shown in Fig. 2 has been fabricated and tested. The essential difference to the original structure (Fig. 1) is that the capacitance of the gate with respect to source is significantly smaller than that of the "grounded gate" structure shown in Fig. 1.

Electrical Characteristics

The low field DC resistance of the devices fabricated during this (third) period of the contract varied between 17 and 60 Ohms in very good agreement with precalculated values. All devices are 400 μm wide.

RF data have been taken in both the stable amplifier mode and in the oscillator mode.

a) Broadband amplification

Samples with overlapping gate electrode (Fig. 1) have been operated as stable amplifiers in a circuit configuration as shown in Fig. 3 with the dielectric resonator removed. The FECTED is mounted at the end of the 50 Ohm stripline with two radial line stubs connected to gate and source via $\lambda/2$ line sections providing RF ground potential to both gate and source. Fig. 4 shows both input power P_{in} and output power P_{out} versus frequency with several db of gain. 5db of gain compression occurred at this power level and a maximum gain of 10db was obtained when P_{in} was reduced by a factor of 10. Drain and gate voltages were 6.8V and -4.2V, respectively. The DC drain current was 120mA. Very low gain has been measured around 37 GHz.

b) 30 GHz oszillations

When a 28 GHz dielectric resonator was placed near the drain end of the device oscillations with a maximum output power of 10mw have been observed at 29.7 GHz with 1.2 % DC to RF conversion efficiency. The frequency of oscillation could be changed by 100 MHz with 1db power output reduction by changing the gate bias voltage by a few tenths of a volt.

Devices with finger gate produced only 1mw with 0.1 % efficiency.

c) 37 GHz oscillations

Both types of devices have been operated as oscillators at 37 GHz with only 0.1 % efficiency. Since lower frequency oscillations were absent, the low efficiency can be explained only by poor circuit matching at this frequency.

Conclusions and Future Research Plan

FECTED's have for the first time produced fundamental frequency oscillations at non-transit-time related frequencies with efficiencies greater than 1 % : 10mw at 30 GHz and several db of reflection gain between 26 and 30 GHz have been obtained. Since computer simulations predict 2 - 5 times higher values over full Ka-band future work during the next contract period (September 87-February 88) will concentrate on further optimizing stripline circuitry including GaAs varactor diodes connected in parallel to the device, minimizing parasitic reactances caused by long bonding wires and reducing the gate length. Gate length reduction down to submicrometer dimensions could possibly increase efficiency as the DC power consumed underneath the gate is lower in a shorter gate region.

Personnel

Dr. Kurt Lübke, Helmut Scheiber, Thomas Neugebauer, Christoph Schönherr, Gabriele Roitmayr and Johann Katzenmayer.

Annex

The amount of unused funds remaining on the contract at the end of the period covered by the report is $ 64,880.00 minus $ 5,880.00 for which an invoice has been submitted in September, 1987.

Fig.1
Cross sectional view of a FECTED with overlapping gate

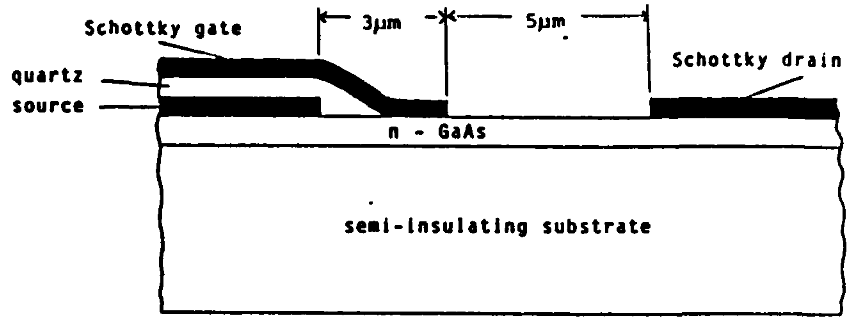


Fig.2
Cross sectional view of a FECTED with finger gate

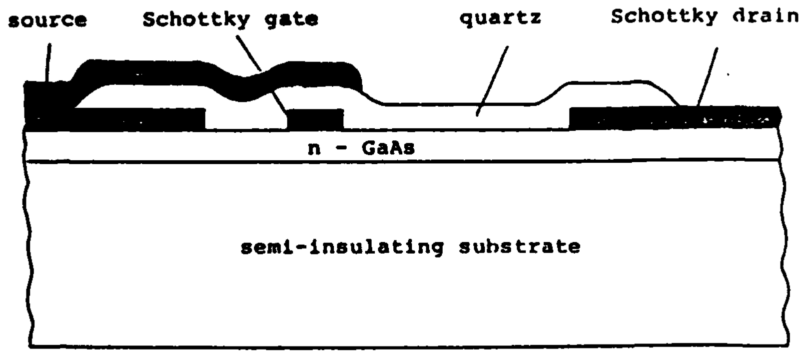


Fig.3
Microstrip circuit configuration of a FECTED oscillator

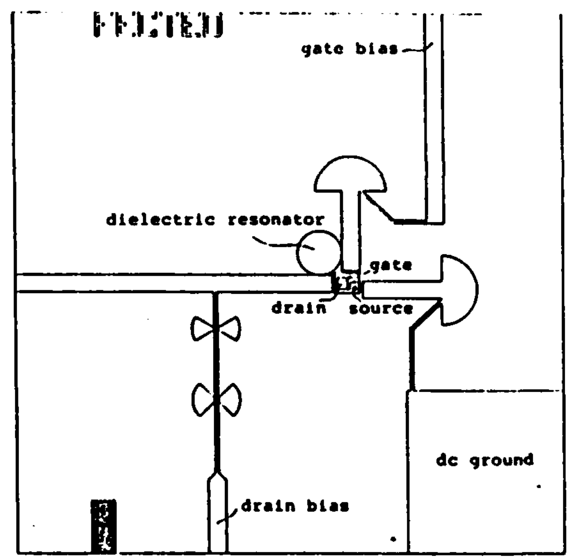
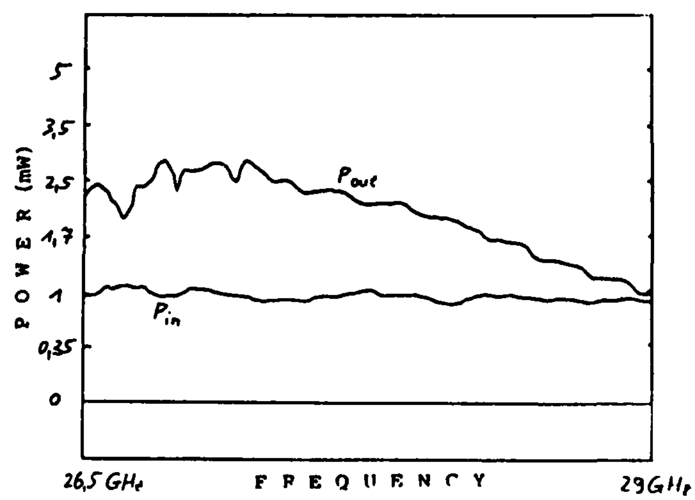


Fig.4
Input power P_{in} and output power P_{out} versus frequency of a FECTED reflection type amplifier



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